Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLR1**
2. **D1**
3. **CLK1**
4. **PR1**
5. **Q1**
6. **N. Q1**
7. **GND**
8. **N. Q2**
9. **Q2**
10. **PR2**
11. **CLK2**
12. **D2**
13. **CLR2**
14. **VCC**

**10**

**11**

**9 8 7 6 5**

**4**

**3**

**12 13 14 1 2**

**U74Y**

**MASK**

**REF**

**.025”**

**.025”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003”**

**Backside Potential: GND**

**Mask Ref: U74Y**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 4/17/17**

**MFG: FAIRCHILD THICKNESS .0135” P/N: 54HC74**

**DG 10.1.2**

#### Rev B, 7/1